REMARKS

Applicants respectfully request reconsideration of the present U.S. Patent application. Claim 14 has been amended to more clearly define Applicants' invention and was not amended because of the references cited in an Office Action. The amendment to claim 14 is supported by the originally filed claim 14 and in the specification on page 15, lines 19-23. Applicants submit, therefore, that no new matter has been added. Claims 13-16, 19, 20, 22-24 and 26-28 are pending.

REJECTIONS UNDER 35 U.S.C. § 103(a)

Claims 13, 14, and 26 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,652,823 issued to Eto, et al. (*Eto*) in view of U.S. Patent No. 5,337,086 issued to Fujinami (*Fujinami*). For at least the reasons set forth below, Applicants submit that claims 13, 14, and 26 are not rendered obvious in view of *Eto* and *Fujinami*.

The Manual of Patent Examining Procedure ("MPEP"), in § 706.02(j), states:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must be both found in the prior art and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Thus, the MPEP and applicable case law require that a combination of references teach or suggest all of the claim limitations of rejected claims as well as provide motivation for the combination, to sustain an obviousness rejection under 35 U.S.C. § 103.

Claim 14 states:

> ...a memory coupled to the command stream controller and to the write address generator, the memory to store pixel data in a **first order** determined by the write address generator...
>
> a read address generator coupled to the processing circuitry and to the memory, the read address generator to cause the memory to **output pixel data in a second order, wherein the second order comprises a sub-block-by-sub-block row major order**.

(Emphasis added). Applicants' invention is directed toward a method and apparatus for performing motion compensation with a texture mapping engine. In one embodiment of the invention, a write address generator causes pixel data to be stored in a memory in a first order. See, e.g., page 11, lines 8-10. Pixel data is read out from memory sub-block-by-sub-block in row major order. Reading the pixel data in this order optimizes the performance of the memory. See page 15, lines 19-23. Claim 13 depends from 14 and therefore contains the same limitations as claim 14. Claim 26 similarly recites a memory to store pixel data in a first order and read out pixel data from memory in a sub-block-by-sub-block row major order.

Eto states:

> ...a forward direction motion compensating circuit 409 for reading the **macroblock data** of the **frame memory** indicated by the motion vector data supplied thereto from the system controller 414 and **supplying the thus read out macroblock data** to a switching circuit 412 as motion-compensated macroblock data...

See column 10, lines 19-24 (Emphasis added). Thus, *Eto* discloses reading and transferring **macroblocks of data from frame memory**. *Eto* does <u>not</u> however, teach or suggest a memory to store pixel data in a first order and read out pixel data from memory in a second order where the second order is sub-block-by-sub-block in row major order.

Fujinami is cited as teaching that macroblocks are divided into sub-blocks and the use of a read address generator for the selection of sub-blocks. The Office Action directs the applicants attention to column 4, lines 39-52. *Fujinami* discloses:

> The **image data** divided into macroblocks and further into subblocks as shown in FIG. 3 are stored in the frame memory 1 block by block. The data of each subblock thus stored in frame memory 1 is read out therefrom...

See column 4, lines 40-44 (emphasis added). Thus, *Fujinami* discloses dividing **image data** into macroblocks and further into sub-blocks. *Fujinami* does not, however, teach or suggest a memory to **store pixel data in a first order** and **read out pixel data from memory in a second order that is sub-block-by-sub-block in row major order**. *Fujinami*, therefore, cannot cure the deficiencies of *Eto*.

As shown above, neither *Eto* nor *Fujinami* teach or suggest a memory to store pixel data in a first order and read out pixel data from memory in a second order that is sub-block-by-sub-block in row major order as claimed by Applicants. Thus, no combination of *Eto* with *Fujinami* teaches or suggests a memory to store pixel data in a first order and read out pixel data from memory in a second order that is sub-block-by-sub-block in row major order. For at least the reason that neither reference, alone or in combination, teaches or suggests the two orderings as claimed, Applicants respectfully submit that no combination of *Eto* with *Fujinami* renders claims 13, 14, and 26 obvious.

Claims 15, 16, 27, and 28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Eto* in view of *Fujinami*, and in further view of U.S. Patent No. 5,892,518 issued to Mizobata et. al. (*Mizobata*). Claims 15 and 16 depend from claim 14. Claims 27 and 28 depend from claim 26. For at least the reasons set forth below, Applicants submit that claims 15, 16, 27, and 28 are not rendered obvious by *Eto*, *Fujinami*, and *Mizobata*.

Mizobata is cited to teach "a setup engine that determines a bounding box for pixels manipulated by the instruction, wherein the bounding box contains all edges of a macroblock and wherein processing circuitry comprises a windower having a first mode wherein pixels inside a triangle within a bounding box are processed and a second mode wherein all pixels within the

bounding are processed." Whether or not *Mizobata* discloses the limitations cited by the Office Action, it does not teach or suggest a memory to store pixel data in a first order and read out pixel data from memory in a second order that is sub-block-by-sub-block in row major order. Thus, Applicants respectfully submit that no combination of *Eto*, *Fujinami*, and *Mizobata* renders claims 15, 16, 27, and 28 obvious.

Claims 20, 22, and 23 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Eto*, in view of *Fujinami*, and in further view of U.S. Patent No. 6,208,350 B1 issued to Herrera (*Herrera*). Claims 22 and 23 depend from claim 20. For at least the reasons set forth below, Applicants submit that claims 20, 22, and 23 are not rendered obvious in view of *Eto*, *Fujinami*, and *Herrera*.

Claim 20 recites:

> a memory coupled to the command stream controller, the memory to store **pixel data** related to a macroblock in a **first order,** the first order is based on output from an Inverse Discrete Cosine Transform (IDCT) operation...
>
> a read address generator coupled to the memory, the read address generator to cause the memory to **output the pixel data** related to a macroblock in a **second order**, the read address generator to cause the memory to output pixel data in **sub-block-by-sub-block row major order**...

Thus, Applicants claim an apparatus that stores pixel data into a memory in a first order that is based on the output of an IDCT operation and a read address generator that outputs pixel data in a second order that is sub-block-by-sub-block in row major order. As stated above, the MPEP and applicable case law require that a combination of references teach or suggest all of the claim limitations of rejected claims as well as provide motivation for the combination, to sustain an obviousness rejection under 35 U.S.C. § 103.

Herrera is cited as teaching "conventional texture mapping operations and bilinear filterings within motion compensation systems." Whether or not *Herrera* discloses the

limitations cited by the Office Action, it does not teach or suggest a memory to store pixel data in a first order and read out pixel data from memory in a second order that is sub-block-by-sub-block in row major order. Thus, Applicants respectfully submit that no combination of *Eto*, *Fujinami*, and *Herrera* renders claim 20 obvious.

Applicants further submit that there is no suggestion or motivation to combine *Herrera* with *Eto*. MPEP § 2143.01 states:

> Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art.

The teaching or suggestion to make the claimed combination must be found in the prior art, not in Applicants' disclosure. *See In re Vaeck*, 20 USPQ2d 1438 (Fed. Cir. 1991). The Office Action does not cite an explicit suggestion or motivation to combine *Herrera* with *Eto* and, therefore, if the suggestion exists, it must be implicit.

Eto discloses an apparatus that performs video encoding and video decoding. See, e.g., FIG. 1 and FIG. 7. *Herrera*, in contrast, discloses a combination of a modified graphics accelerator with software to create a cost effective hybrid solution to providing a personal computer with DVD capabilities. See, e.g., column 4, lines 63-66 and FIG. 8. *Herrera* states:

> The second type of solution, places the DVD processing task entirely on the PC's hardware ... providing such specialized circuitry (**e.g., a DVD decoder**) can be very expensive and result in significantly increased costs, which can be **devastating** in the highly competitive PC market. The specialized circuitry can also **reduce the performance of the PC** by requiring access to the PC's bus(es), interfaces and memory components, in some PC architectures.

See column 4, lines 37-46. *Herrera*, therefore, explicitly teaches away from *Eto*, rather than providing an implicit basis to combine the references. Because *Herrera* explicitly teaches away from *Eto*, Applicants respectfully submit that the combination of *Herrera* with *Eto* is improper.

Claims 22 and 23 depend from claim 20. Because dependent claims include the limitations of the claims from which they depend, Applicants submit that claims 22 and 23 are not rendered obvious by *Eto*, *Fujinami*, and *Herrera*.

Claim 24 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Eto*, in view of *Fujinami*, in view of *Herrera*, and in further view of U.S. Patent No. 5,446,495 issued to Tourtier,et al. (*Tourtier*). For at least the reasons set forth below, Applicants submit that claim 24 is not rendered obvious in view of *Eto*, *Fujinami*, *Herrera*, and *Tourtier*.

Tourtier is cited as teaching "the particular motion compensation pipeline processings and multiple frame prediction operations" claimed by Applicants. Whether or not *Tourtier* discloses the limitations cited by the Office Action, it does not teach or suggest a memory to store pixel data in a first order and read out pixel data from memory in a second order that is sub-block-by-sub-block in row major order. Thus, Applicants respectfully submit that no combination of *Eto*, *Fujinami*, *Herrera*, and *Tourtier* renders claim 24 obvious.

Claims 19 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Eto*, in view of *Fujinami*, and in further view of *Tourtier*. For at least the reasons set forth below, Applicants submit that claim 19 is not rendered obvious in view of *Eto*, *Fujinami*, and *Tourtier*.

As discussed above, whether or not *Tourtier* discloses the limitations cited by the Office Action, it does not teach or suggest a memory to store pixel data in a first order and read out pixel data from memory in a second order that is sub-block-by-sub-block in row major order. Thus, Applicants respectfully submit that no combination of *Eto*, *Fujinami*, and *Tourtier* renders claim 19 obvious.

CONCLUSION

For at least the foregoing reasons, Applicants submit that the rejections have been overcome. Therefore, claims 13-16, 19, 20, 22-24 and 26-28 are in condition for allowance and such action is earnestly solicited. The Examiner is respectfully requested to contact the undersigned by telephone if such contact would further the examination of the present application.

Please charge any shortages and credit any overcharges to our Deposit Account number 02-2666.

Respectfully submitted,
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Catherine Lauthan 5/9/02
Signature Date

MARKED VERSION OF THE AMENDED CLAIM

14. (Amended) A circuit for generating motion compensated video, the circuit comprising:

a command stream controller coupled to receive an instruction to manipulate motion compensated video data;

a write address generator coupled to the command stream controller;

a memory coupled to the command stream controller and to the write address generator, the memory to store pixel data in a first order determined by the write address generator;

processing circuitry coupled to the write address generator to receive control information and data from the command stream controller to generate a reconstructed video frame; and

a read address generator coupled to the processing circuitry and to the memory, the read address generator to cause the memory to output pixel data in a second order, wherein the second order comprises a sub-block-by-sub-block row major order.